

SW side

Copy data from buffer1
Read missing data counter of buffer1
Clear fill flag and missing counter of buffer1

Clear buffer1
fill flag

Check buffer1 fill
flag

Start

Map memory/Init
decimation

Reset buffers states
Clear overflow counter
Clear fill buffer flag

Buffer1 is filled

Set flag filled
buffer1

Write
buffer1 from
ADC

Buffer2 filled
flag is set

Buffer2 filled
flag is set

Increase
buffer1 missing data
counter

Buffer2 filled
flag is clear

Buffer1 filled
flag is clear

Buffer1 filled
flag is clear

FPGA side

Buffer2 filled
flag is clear

Increase
buffer2 missing data
counter

Buffer1 filled
flag is set

Buffer1 filled
flag is set

Write
buffer2 from
ADC

Buffer2 is filled

Set flag filled
buffer2

Check buffer2 fill
flag

Clear buffer2
fill flag

Copy data from buffer2
Read missing data counter of
buffer2
Clear fill flag and missing counter
of buffer2

SW side

Global registers:

- Start / Stop recording (R/W)
- Reset all flags and states (W)

Common registers (flags) for two channels:

- Buffer 1 full (R)
- Buffer 2 full (R)
- Number of lost data on buffer 1 (R)
- Number of lost data on buffer 2 (R)
- Clear buffer 1 fill flag and lost data counter (W)
- Clear buffer 2 fill flag and lost data counter (W)