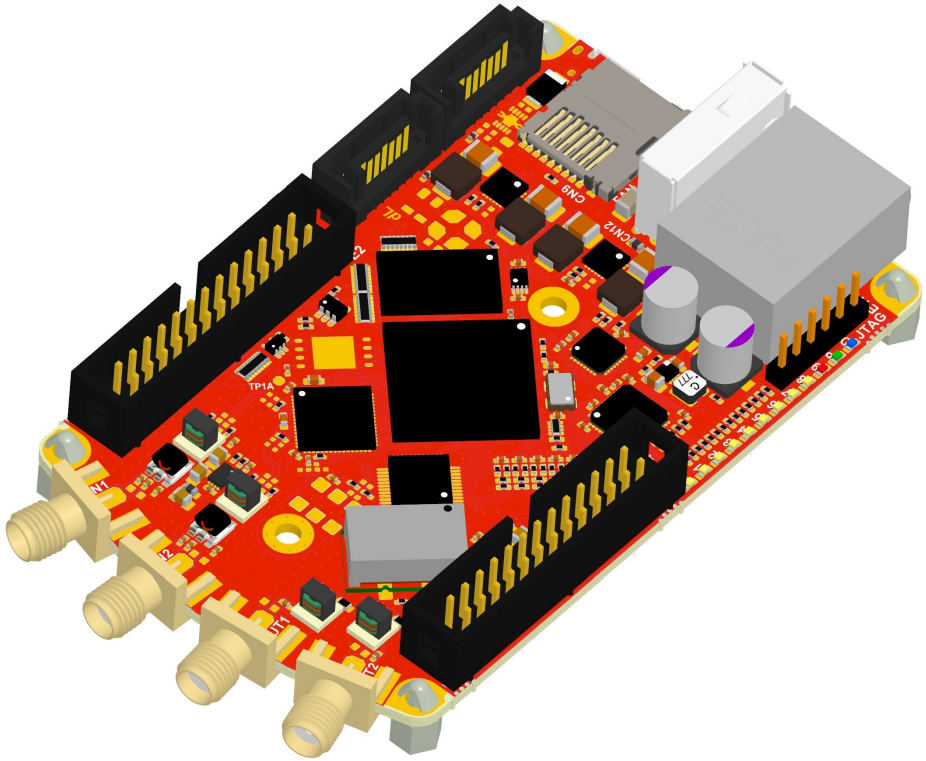



**Red Pitaya d.o.o.**
**Velika pot 22**
**5250 Solkan**
**Slovenia**

**www.redpitaya.com**


## *Electrical schematics for:*

***name:*** ***STEM122-16SDR***

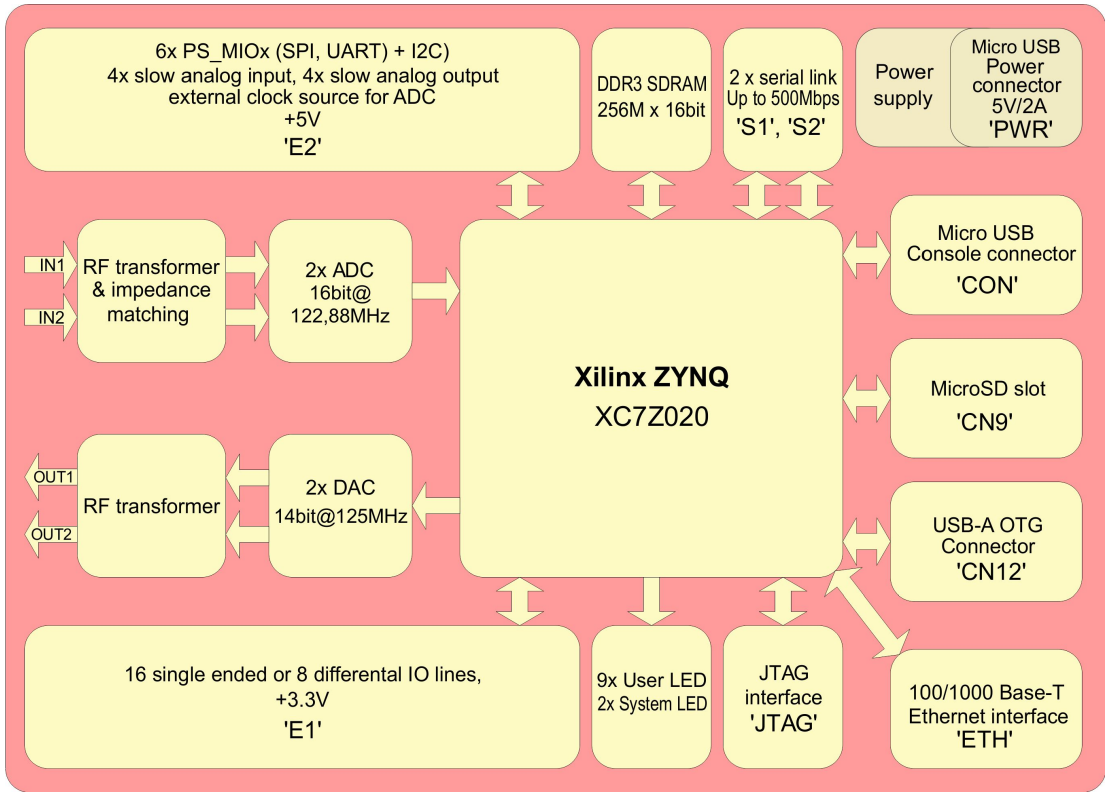
***version:*** ***V1r1***

***variant:*** ***Series1***



| | | | | | |
|---|---|---|---|---|---|
| Designer: | Redpitaya | Document: | Document_Name | Sheet 1 of 9 | |
| Drawn By: | IT015 | Modif. Date: | 15. 10. 2019 | SCHEMATIC | |
| Approved By: | IT004 | Print Date: | 15. 10. 2019 | Size: A4 H | |

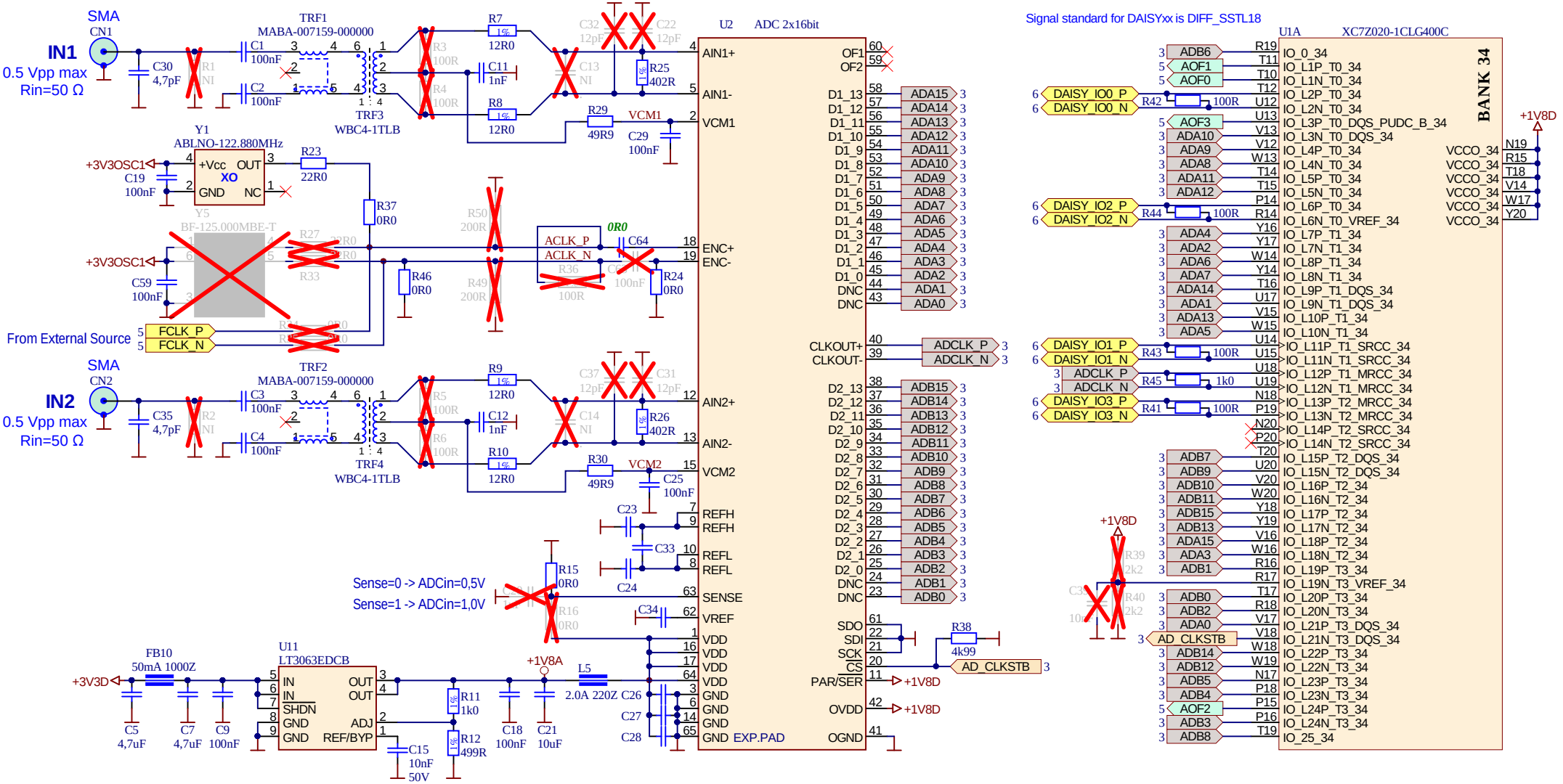
**Red Pitaya Software Defined Radio**




| | | | | | |
|---|---|---|---|---|---|
| Designer: | Redpitaya | Document: | Document_Name | Sheet 2 of 9 | |
| Drawn By: | IT015 | Modif. Date: | 15. 10. 2019 | SCHEMATIC | |
| Approved By: | IT004 | Print Date: | 15. 10. 2019 | Size: A4 H | |

**STEM122-16SDR V1r1 block schematics**

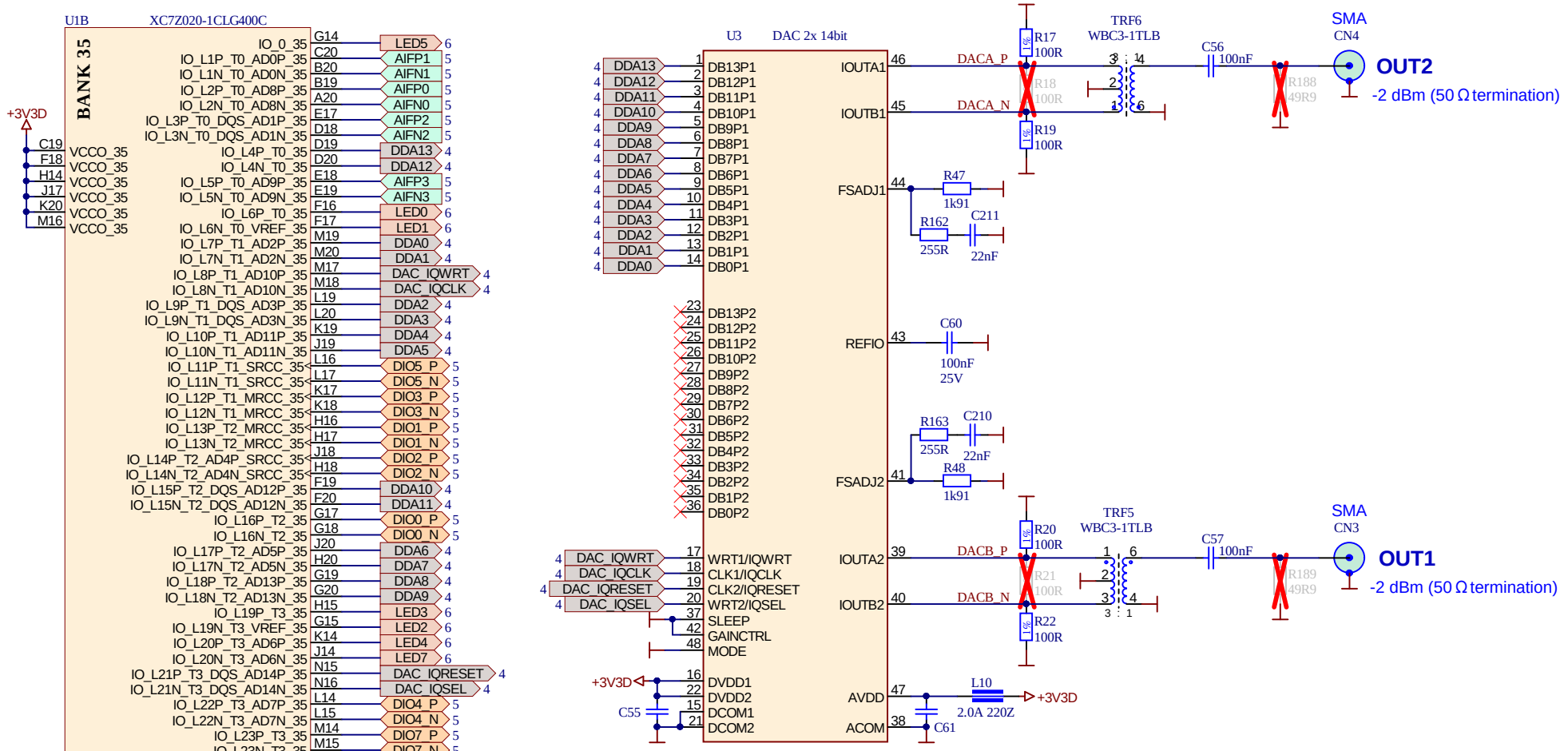
redpitaya




| | | | | | |
|---|---|---|---|---|---|
| Designer: | Redpitaya | Document: | Document_Name | Sheet 3 of 9 | |
| Drawn By: | IT015 | Modif. Date: | 15. 10. 2019 | SCHEMATIC | |
| Approved By: | IT004 | Print Date: | 15. 10. 2019 | Size: A4 H | |

**Analog front-end and analog-digital converter, FPGA bank 34**

redpitaya




Note: number next to port symbol indicates the sheet where the signal is connected

| | | | | |
|---|---|---|---|---|
| Designer: | Redpitaya | Document: | Document_Name | Sheet 4 of 9 |
| Drawn By: | IT015 | Modif. Date: | 15. 10. 2019 | SCHEMATIC |
| Approved By: | IT004 | Print Date: | 15. 10. 2019 | Size: A4 H |

# Analog back-end and digital-analog converter, FPGA bank 35

redpitaya

PS_MIO08 is output only and at power-up must be low level (no external pull-ups)!

22 single ended or
11 differential digital I/O
with 3,3V logic levels

## E2

CN5

+5V DC
NC
PS_MIO10
PS_MIO11
PS_MIO12
PS_MIO13
Output only! PS_MIO08
PS_MIO09
I2C0 SCL
I2C0 SDA
Ext com.mode (0~+0,5V)
GND
Analog Input 0
Analog Input 1
Analog Input 2
Analog Input 3
Analog Output 0
Analog Output 1
Analog Output 2
Analog Output 3
GND
GND
Ext Adc CLK+
Ext Adc CLK-
GND
GND

PS_MIO10 7 (SPI1_MOSI)
PS_MIO11 7 (SPI1_MISO)
PS_MIO12 7 (SPI1_SCK)
PS_MIO13 7 (SPI1_CS#)
PS_MIO08 7 (TxD1)
PS_MIO09 7 (RxD1)
I2C0_SCL 7
I2C0_SDA 7

AIcm
C238 470nF

AI0 5
AI1 5
AI2 5
AI3 5
AO0 5
AO1 5
AO2 5
AO3 5

FCLK_P 3
FCLK_N 3

IDC 2.54mm 26 pin low profile

0~+3,5Vin

0~+1,8Vout

LVDS signal level

(alternative ZYNQ function)
3,3V logic levels

0,5V XADC range

AI0 R85 30k0 R89 4k99 R93 1k0 C101 220pF AIFP0 4
AIFN0 4 R94 1k0
AI1 R86 30k0 R90 4k99 R95 1k0 C102 220pF AIFP1 4
AIFN1 4 R96 1k0
AI2 R87 30k0 R91 4k99 R97 1k0 C103 220pF AIFP2 4
AIFN2 4 R98 1k0
AI3 R88 30k0 R92 4k99 R99 1k0 C104 220pF AIFP3 4
AIFN3 4 R100 1k0

Vcm=0V

0R resistor
in place of
capacitor
C237 0R0

U22A

common voltage setup
+0V5ref
R176
XADCREF 6
C242 100nF
R177 1k5
1k0

Remove if
external common mode
voltage is used!

AO0 AO1 AO2 AO3
RA8C 3 14 100R AOF0 3
RA8D 4 13 100R AOF1 3
RA8E 5 12 100R AOF2 3
RA8F 6 11 100R AOF3 3
C96 8,2nF C97 8,2nF C99 8,2nF C100 8,2nF

+5VD R139 56k0 R141 1k0 R140 4k99 C184 10nF AIFP4 6
R142 1k0 AIFN4 6
Power supply voltage monitor
0,5V XADC@6,11Vin

U1H XC7Z020-1CLG400C

BANK 13

+3V3D
T8 VCCO_13
U11 VCCO_13
W7 VCCO_13
Y10 VCCO_13

IO_L6N_T0_VREF_13 V5
IO_L11P_T1_SRCC_13 U7
IO_L11N_T1_SRCC_13 V7
IO_L12P_T1_MRCC_13 T9
IO_L12N_T1_MRCC_13 U10
IO_L13P_T2_MRCC_13 Y7 DIO10_P 5
IO_L13N_T2_MRCC_13 Y6 DIO10_N 5
IO_L14P_T2_SRCC_13 Y9 DIO8_P 5
IO_L14N_T2_SRCC_13 Y8 DIO8_N 5
IO_L15P_T2_DQS_13 V8
IO_L15N_T2_DQS_13 W8
IO_L16P_T2_13 W10
IO_L16N_T2_13 W9
IO_L17P_T2_13 U9
IO_L17N_T2_13 U8
IO_L18P_T2_13 W11
IO_L18N_T2_13 Y11
IO_L19P_T3_13 T5
IO_L19N_T3_VREF_13 U5
IO_L20P_T3_13 Y12 DIO9_P 5
IO_L20N_T3_13 Y13 DIO9_N 5
IO_L21P_T3_DQS_13 V11
IO_L21N_T3_DQS_13 V10
IO_L22P_T3_13 V6
IO_L22N_T3_13 W6

## E1

CN6

+3V3D
+3V3D
PL_DIO0_P
PL_DIO0_N
PL_DIO1_P
PL_DIO1_N
PL_DIO2_P
PL_DIO2_N
PL_DIO3_P
PL_DIO3_N
PL_DIO4_P
PL_DIO4_N
PL_DIO5_P
PL_DIO5_N
PL_DIO6_P
PL_DIO6_N
PL_DIO7_P
PL_DIO7_N
PL_DIO8_P
PL_DIO8_N
PL_DIO9_P
PL_DIO9_N
PL_DIO10_P
PL_DIO10_N
GND
GND

DIO0_P DIO0_N DIO1_P DIO1_N DIO2_P DIO2_N DIO3_P DIO3_N DIO4_P DIO4_N DIO5_P DIO5_N DIO6_P DIO6_N DIO7_P DIO7_N DIO8_P DIO8_N DIO9_P DIO9_N DIO10_P DIO10_N

XC7Z020 only

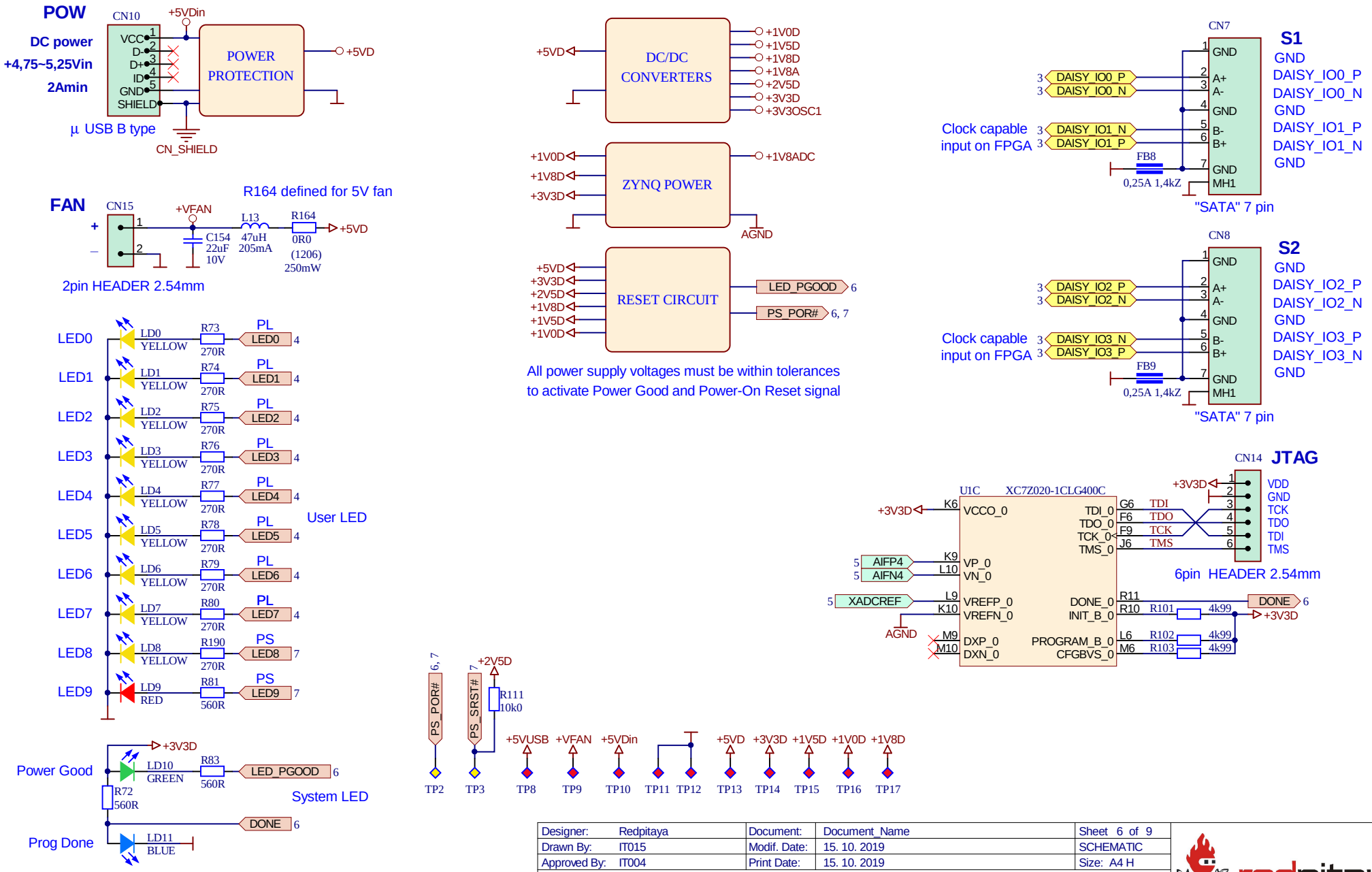
IDC 2.54mm 26 pin low profile

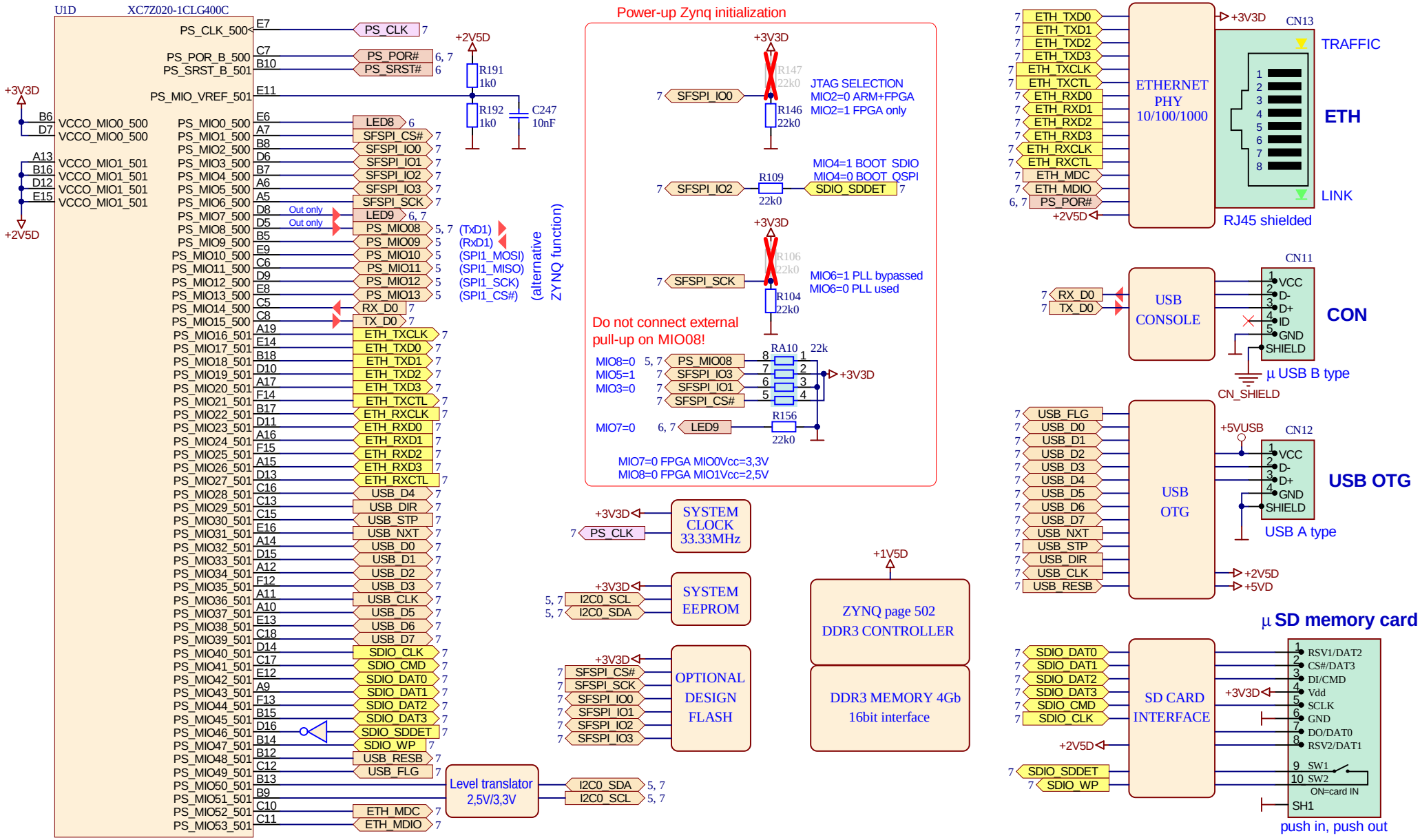
Note: number next to port symbol indicates the sheet where the signal is connected

| | | | | |
|---|---|---|---|---|
| Designer: | Redpitaya | Document: | Document_Name | Sheet 5 of 9 |
| Drawn By: | IT015 | Modif. Date: | 15. 10. 2019 | SCHEMATIC |
| Approved By: | IT004 | Print Date: | 15. 10. 2019 | Size: A4 H |

# I/O digital, I/O slow analog, Extension connectors

redpitaya


POW
DC power
+4,75~5,25Vin
2Amin
CN10
+5VDin
VCC
D-
D+
ID
GND
SHIELD
POWER PROTECTION
+5VD
µ USB B type
CN_SHIELD
FAN
CN15
+VFAN
C154 22uF 10V
L13 47uH 205mA
R164 0R0 (1206) 250mW
+5VD
R164 defined for 5V fan
2pin HEADER 2.54mm
LED0
LED1
LED2
LED3
LED4
LED5
LED6
LED7
LED8
LED9
LD0 YELLOW
LD1 YELLOW
LD2 YELLOW
LD3 YELLOW
LD4 YELLOW
LD5 YELLOW
LD6 YELLOW
LD7 YELLOW
LD8 YELLOW
LD9 RED
R73 270R
R74 270R
R75 270R
R76 270R
R77 270R
R78 270R
R79 270R
R80 270R
R190 270R
R81 560R
PL LED0 4
PL LED1 4
PL LED2 4
PL LED3 4
PL LED4 4
PL LED5 4
PL LED6 4
PL LED7 4
PS LED8 7
PS LED9 7
User LED
Power Good
LD10 GREEN
R83 560R
LED_PGOOD 6
+3V3D
R72 560R
Prog Done
LD11 BLUE
DONE 6
System LED
Note: number next to port symbol indicates the sheet where the signal is connected
+5VD
DC/DC CONVERTERS
+1V0D
+1V5D
+1V8D
+1V8A
+2V5D
+3V3D
+3V3OSC1
+1V0D
+1V8D
+3V3D
ZYNQ POWER
+1V8ADC
AGND
+5VD
+3V3D
+2V5D
+1V8D
+1V5D
+1V0D
RESET CIRCUIT
LED_PGOOD 6
PS_POR# 6, 7
All power supply voltages must be within tolerances
to activate Power Good and Power-On Reset signal
PS_POR# 6, 7
PS_SRST# 7
+2V5D
R111 10k0
TP2
TP3
TP8
TP9
TP10
TP11
TP12
TP13
TP14
TP15
TP16
TP17
+5VUSB
+VFAN
+5VDin
+5VD
+3V3D
+1V5D
+1V0D
+1V8D
CN7
S1
GND
DAISY_IO0_P
DAISY_IO0_N
GND
DAISY_IO1_P
DAISY_IO1_N
GND
Clock capable input on FPGA
FB8 0,25A 1,4kZ
"SATA" 7 pin
CN8
S2
GND
DAISY_IO2_P
DAISY_IO2_N
GND
DAISY_IO3_P
DAISY_IO3_N
GND
Clock capable input on FPGA
FB9 0,25A 1,4kZ
"SATA" 7 pin
U1C
XC7Z020-1CLG400C
VCCO_0
VP_0
VN_0
VREFP_0
VREFN_0
DXP_0
DXN_0
TDI_0
TDO_0
TCK_0
TMS_0
DONE_0
INIT_B_0
PROGRAM_B_0
CFGBVS_0
AIFP4
AIFN4
XADCREF
CN14
JTAG
VDD
GND
TCK
TDO
TDI
TMS
6pin HEADER 2.54mm
R101 4k99
R102 4k99
R103 4k99
DONE 6
Designer: Redpitaya
Drawn By: IT015
Approved By: IT004
Document: Document_Name
Modif. Date: 15. 10. 2019
Print Date: 15. 10. 2019
Sheet 6 of 9
SCHEMATIC
Size: A4 H
LED, Power, Fan, Serial I/O, JTAG, testpoints
redpitaya

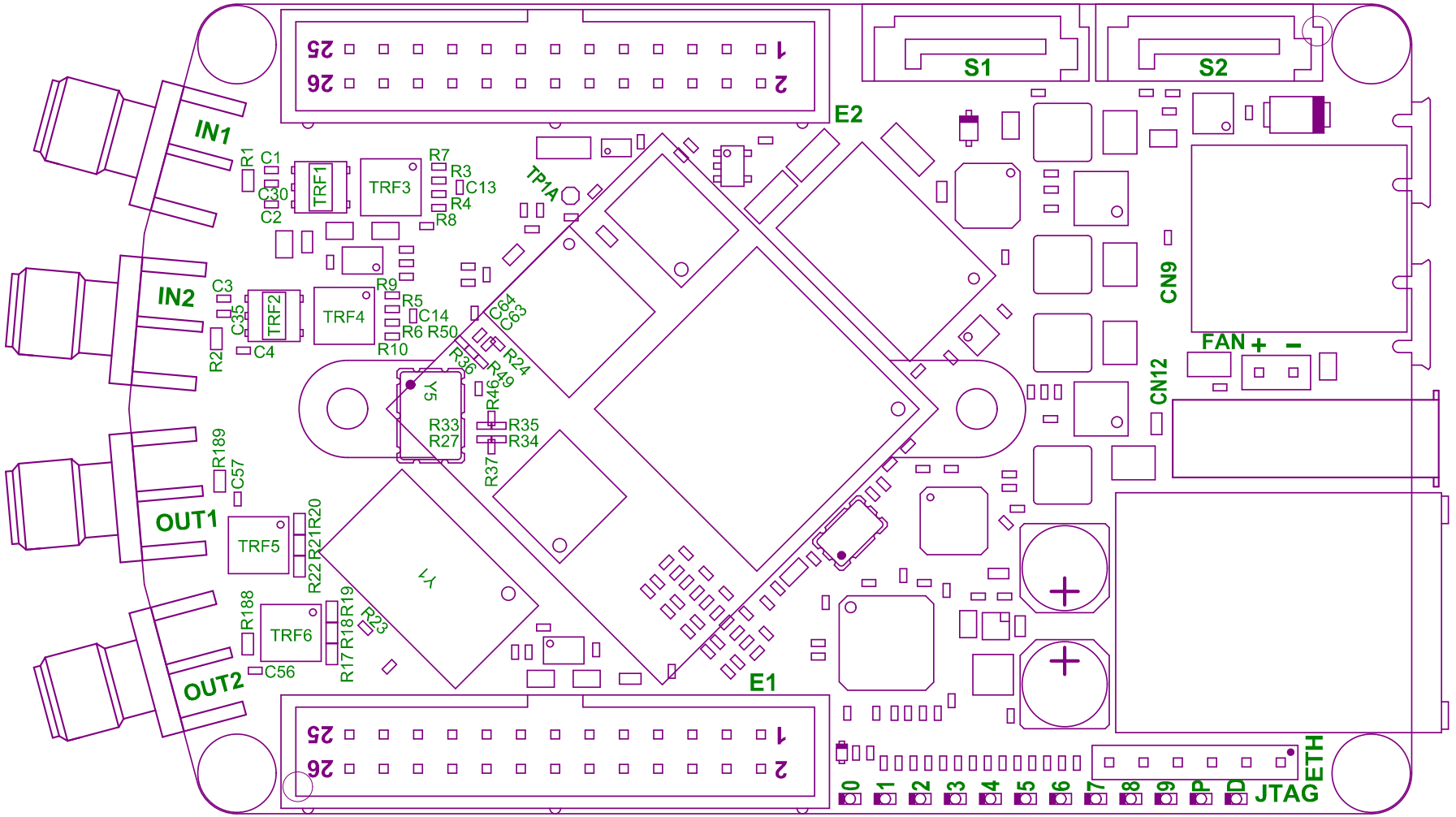



Note: number next to port symbol indicates the sheet where the signal is connected

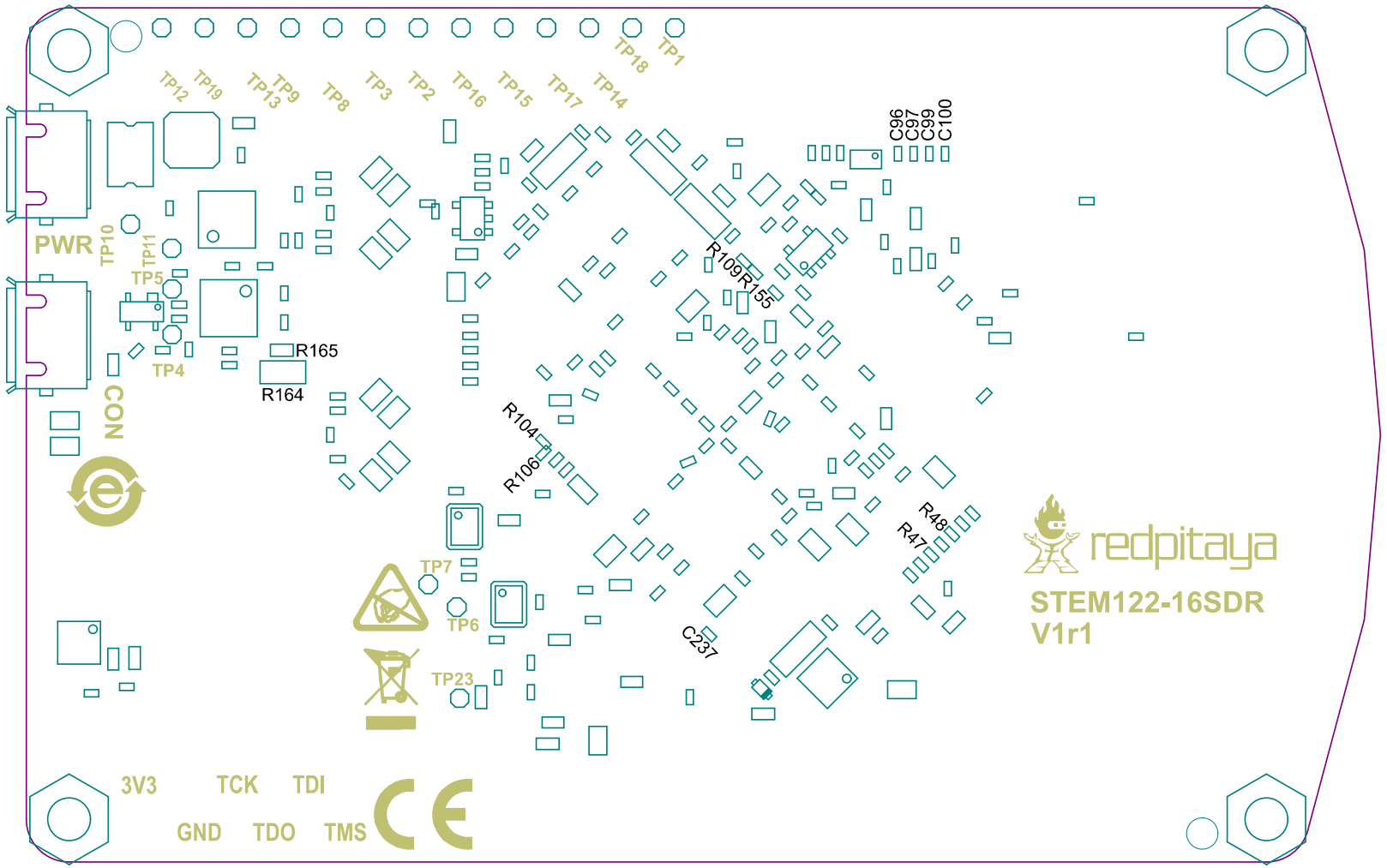
| | | | | |
|---|---|---|---|---|
| Designer: | Redpitaya | Document: | Document_Name | Sheet 7 of 9 |
| Drawn By: | IT015 | Modif. Date: | 15. 10. 2019 | SCHEMATIC |
| Approved By: | IT004 | Print Date: | 15. 10. 2019 | Size: A4 H |

# Zynq PS bank500 and 501, Ethernet, Console, USB, memory

redpitaya




**Assembly top: STEM122-16SDR V1r1**
**- user important components**




**Assembly bottom:STEM122-16SDR V1r1**
**- user important components**