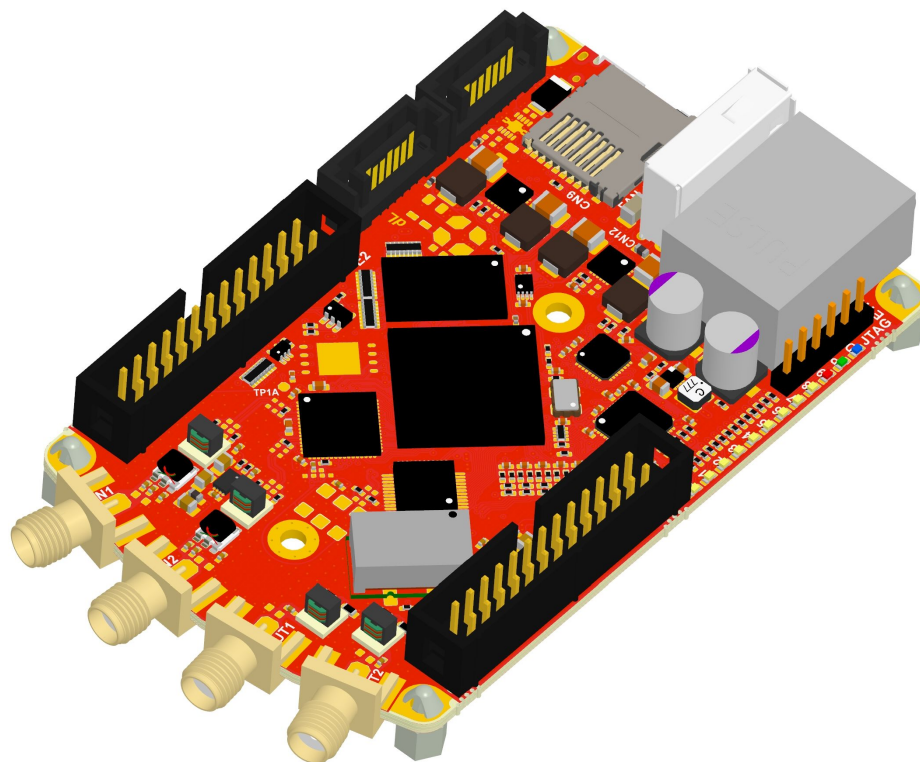




redpitaya

Red Pitaya d.o.o.
Velika pot 22
5250 Solkan
Slovenia

www.redpitaya.com

Electrical schematics for:

name: STEM122-16SDR
version: V1r1
variant: Series1

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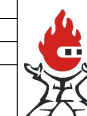
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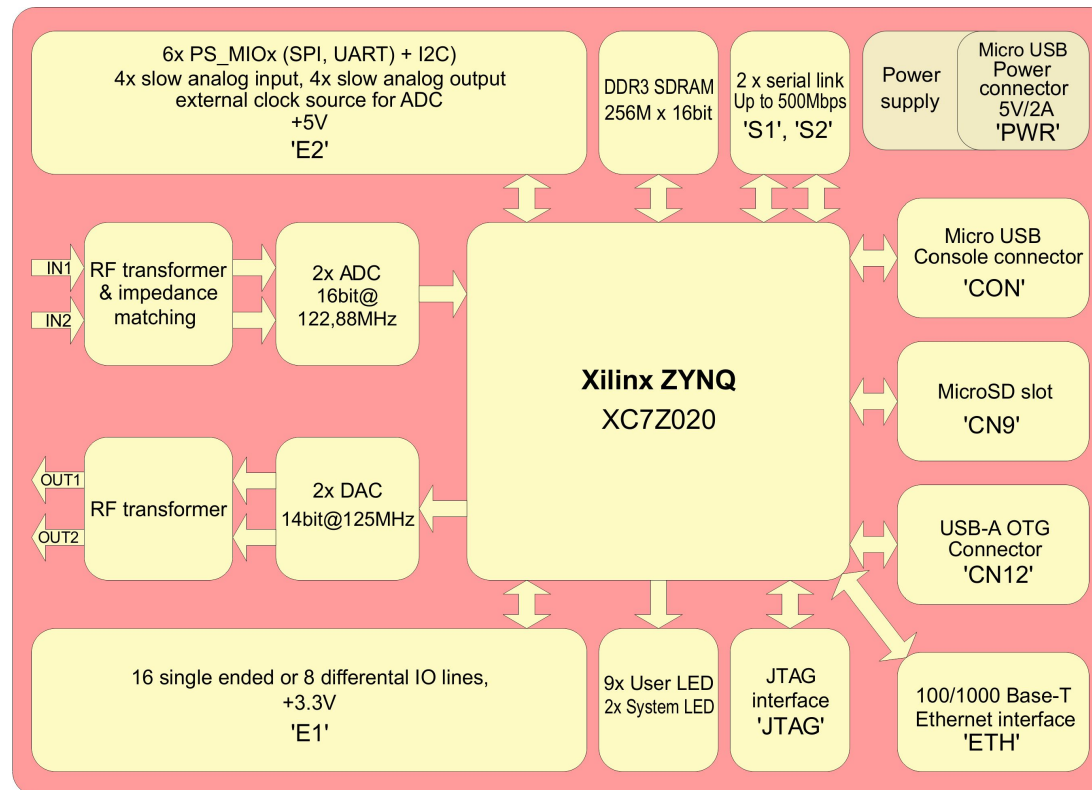
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Red Pitaya Software Defined Radio



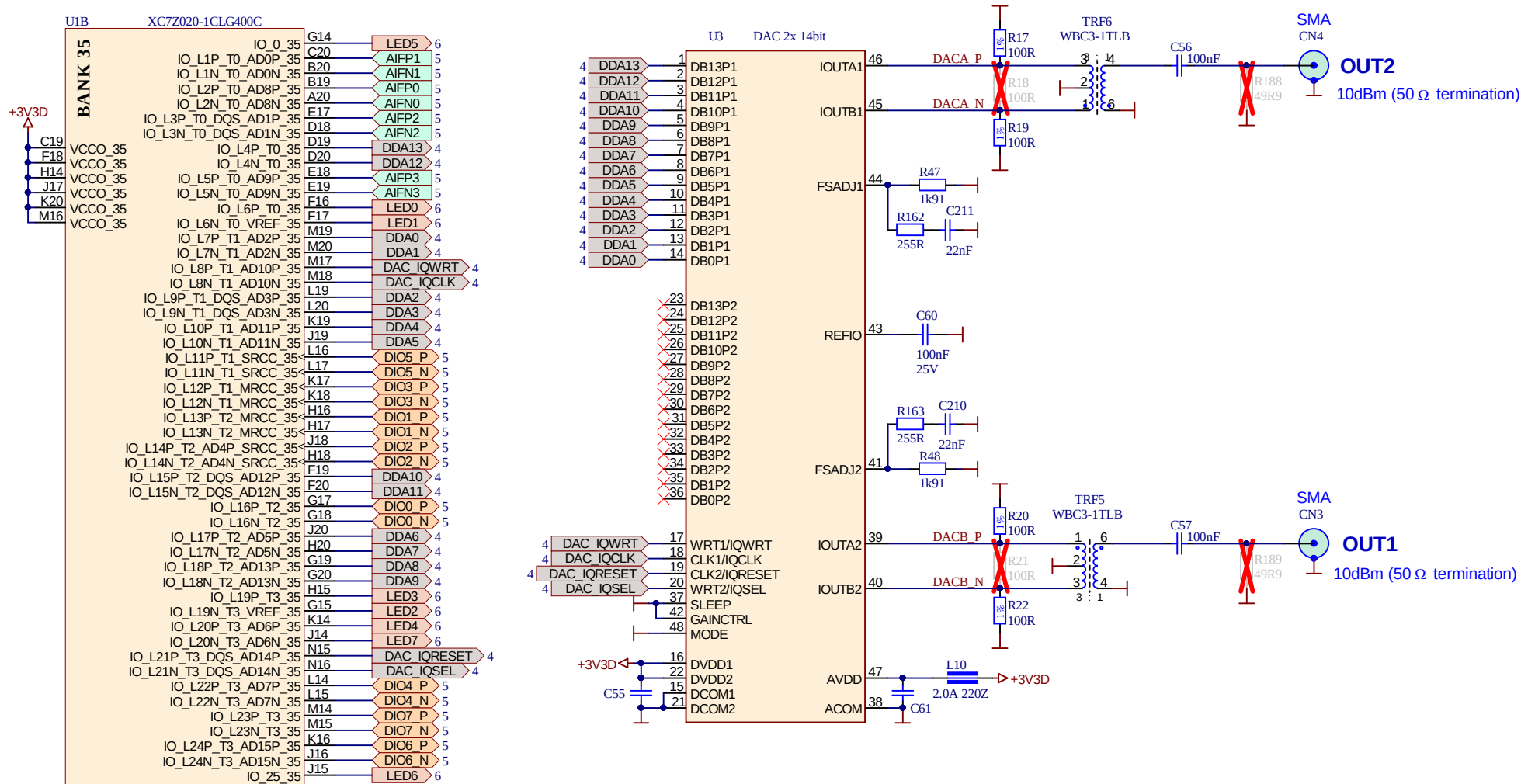
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STEM122-16SDR V1r1 block schematics





Note: number next to port symbol indicates the sheet where the signal is connected

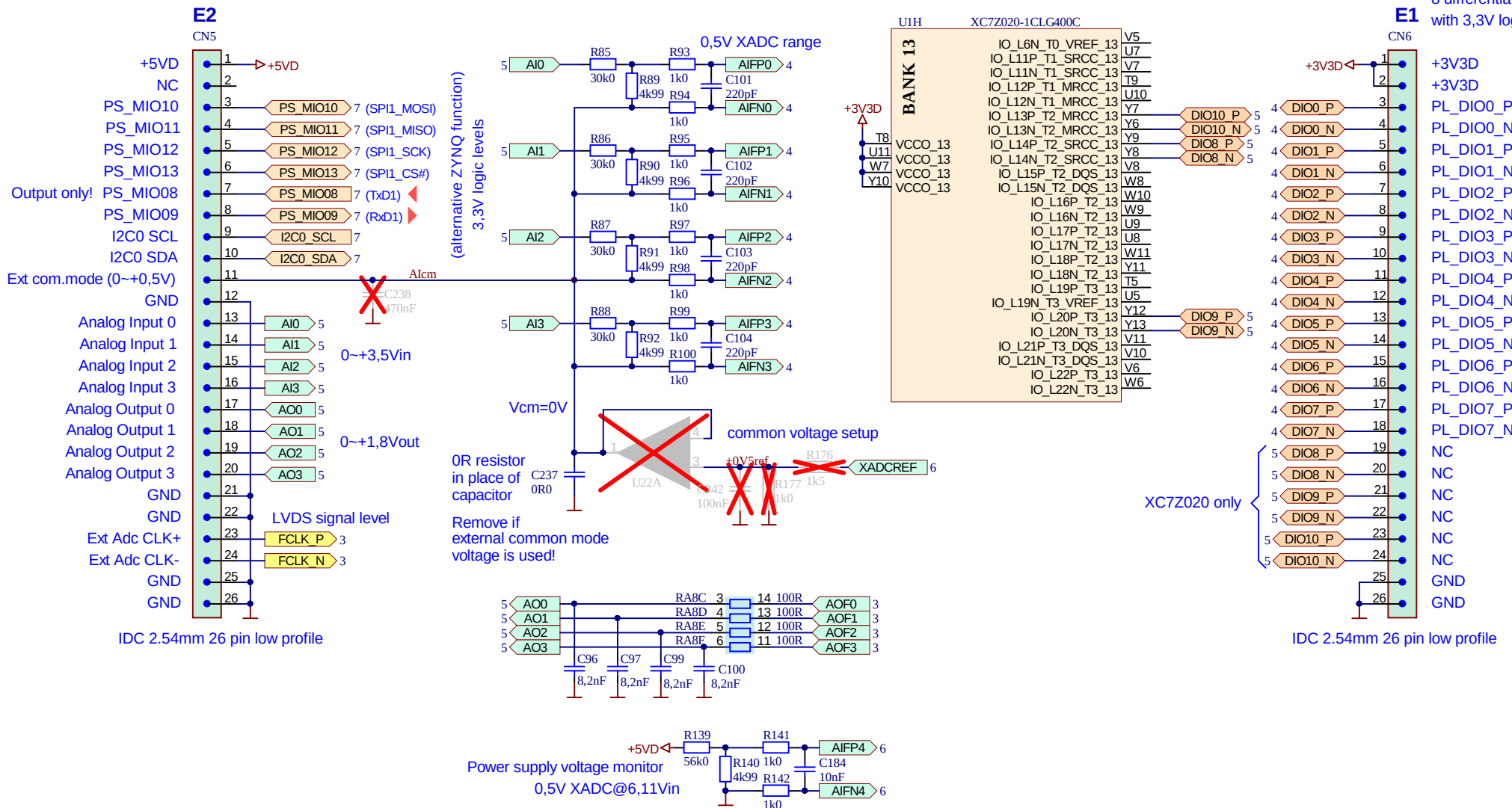
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Analog back-end and digital-analog converter, FPGA bank 35



PS_MIO08 is output only and at power-up must be low level (no external pull-ups)!

16 single ended or
8 differential digital I/O
with 3,3V logic levels

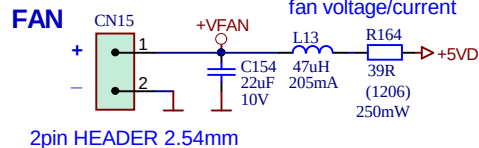
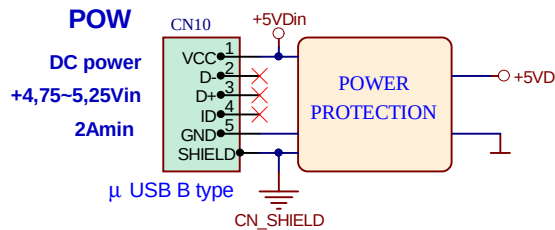


Note: number next to port symbol indicates the sheet where the signal is connected

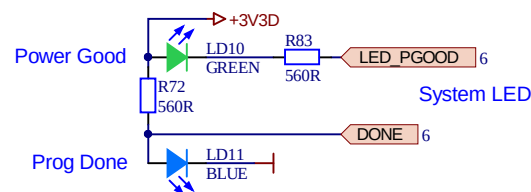
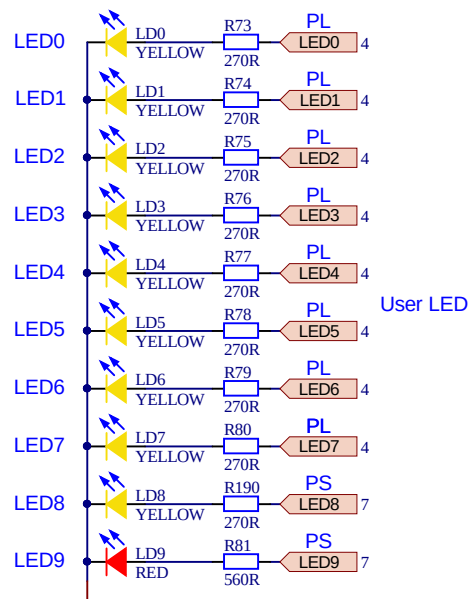
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Approved By: IT004	Print Date: 15. 10. 2019	Size: A4 H

I/O digital, I/O slow analog, Extension connectors

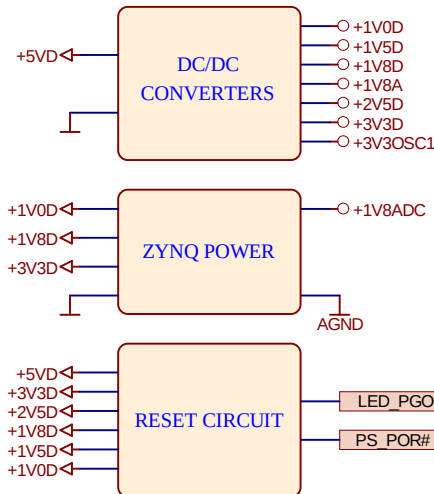




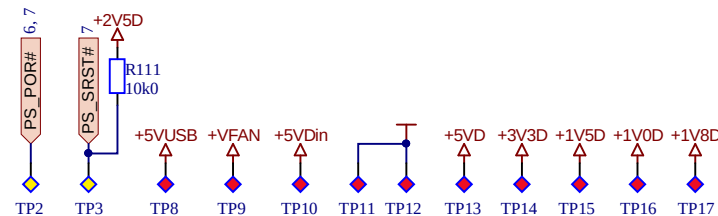
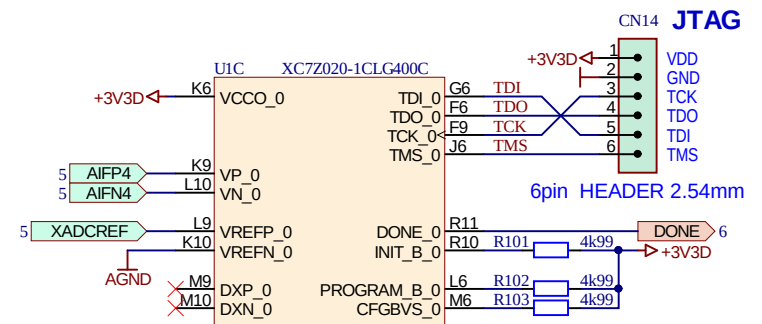
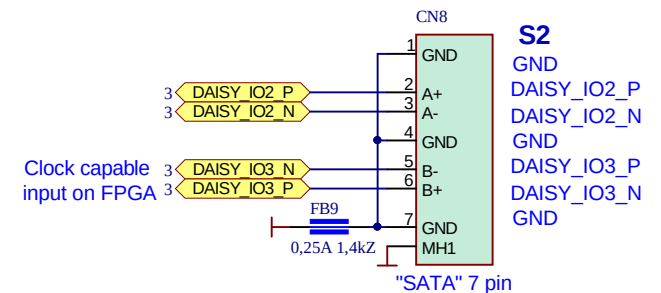
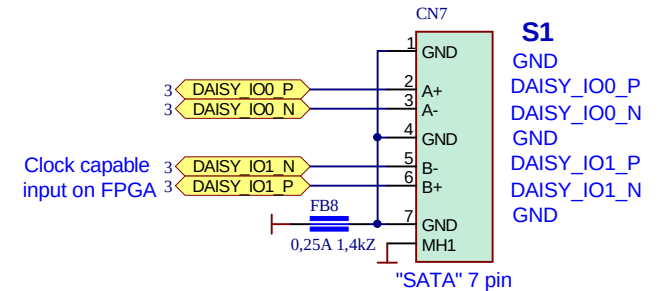
R164 defined for fan 3,3V 40mA,
change resistance for different
fan voltage/current



Note: number next to port symbol indicates the sheet where the signal is connected



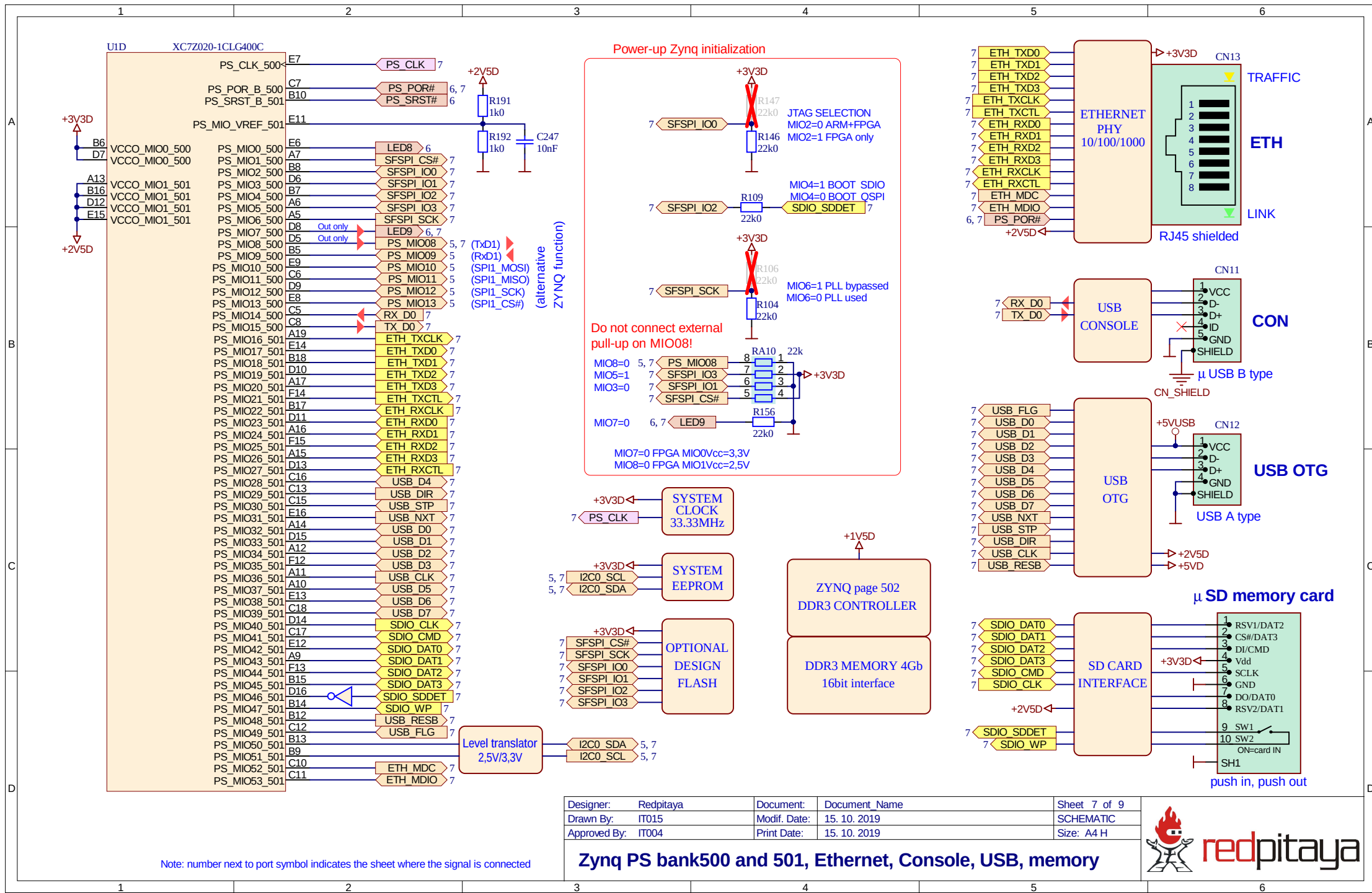
All power supply voltages must be within tolerances
to activate Power Good and Power-On Reset signal



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LED, Power, Fan, Serial I/O, JTAG, testpoints

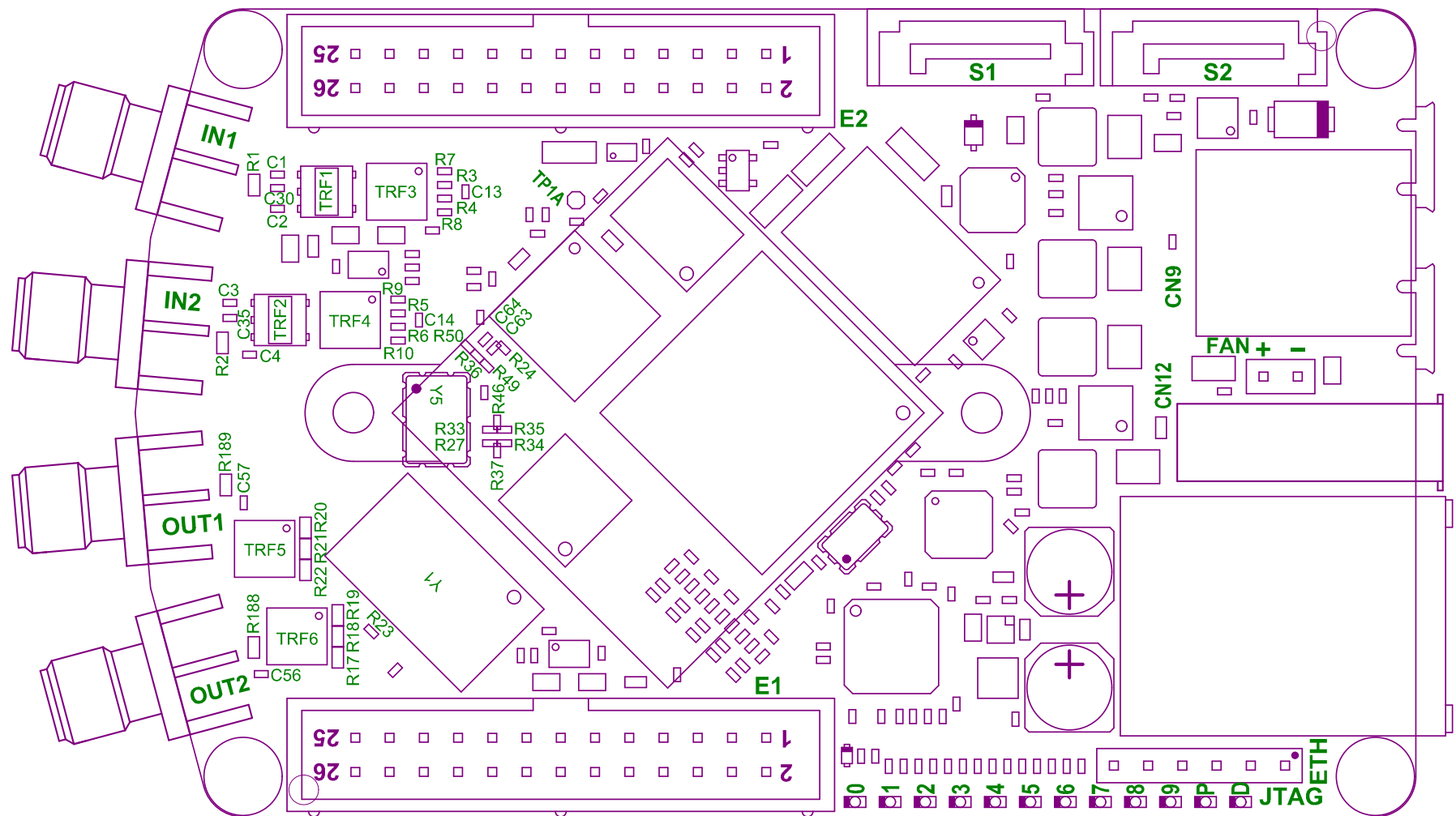




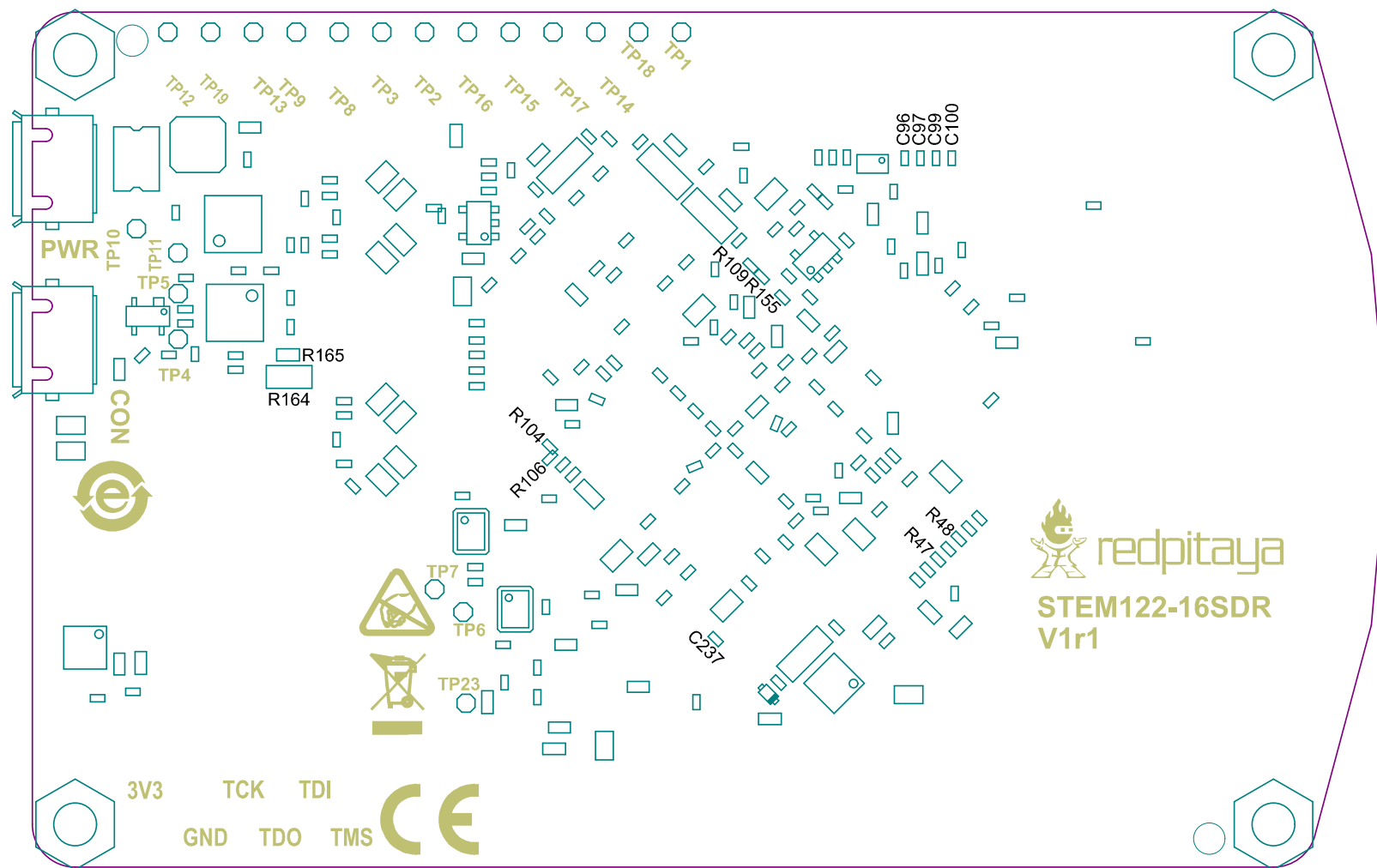
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Zynq PS bank500 and 501, Ethernet, Console, USB, memory





Assembly bottom: STEM122-16SDR V1r1
- user important components



Assembly top: STEM122-16SDR V1r1
- user important components